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APPLICATION

FOR

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TITLE: MULTI-CHIP MODULE WITH EXTENSION

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MULTI-CHIP MODULE WITH EXTENSION

Background

This invention relates generally to multi-chip modules for coupling more than one chip together in a single package.

For a number of reasons, it is desirable to package more than one integrated circuit die or chip in a single package. In some cases, the two dice may necessitate different processing technologies. In such case, the two dice must be made independently and then combined thereafter. For example, one die may be made using a bipolar process and another may be made using a complementary metal oxide semiconductor (CMOS) process. Similarly, one die may use a logic process and the other die may use a memory process. For example, some dice may use stacked gate designs which may be incompatible with logic processes.

Thus, in a variety of situations, it may be desirable to put components in close proximity without making them on the same integrated circuit fabrication process. In addition, in some cases, the level of integration available may be such that to achieve the full capabilities, separate dice must be used. If separate dice are used, it may still be desirable to connect the dice together to the outside

world through a single set of input and output connections. These input and output connections may be, for example, pins or solder balls. In some cases it may be desirable to interconnect the two dice to each other and then to interconnect them together to the outside world.

Thus, there is a need for packages which enable dice to be connected together before connection to the outside world.

Summary

In accordance with one aspect, a multi-chip module includes a laminate layer having a top and a bottom sides and a passage. A first chip is secured to the bottom side of the layer. The first chip is wire bonded to the top side of the layer through the passage. A second chip is secured to the top side of the layer by bumps. The layer includes an extension accessible beyond one of the chips. The extension includes contacts on said bottom side, electrically coupled to said first and second chips.

Other aspects are described in the accompanying specification and claims.

Brief Description of the Drawings

Fig. 1 is a greatly enlarged cross-sectional view of one embodiment of the present invention;

Fig. 2 is a greatly enlarged cross-sectional view of a subassembly, in accordance with the embodiment shown in

Fig. 1, after a first chip has been connected to a laminate layer and the assembly wire bonded;

Fig. 3 is a greatly enlarged cross-sectional view of the embodiment shown in Fig. 2 after a second chip has been attached;

Fig. 4 is a greatly enlarged cross-sectional view of the package of Fig. 3 after it has been subject to encapsulation;

Fig. 5 is a greatly enlarged bottom plan view of one embodiment of the present invention; and

Fig. 6 is a greatly enlarged bottom plan view of another embodiment of the present invention.

Detailed Description

Referring to Fig. 1, a multi-chip module 10 includes a first chip 16, a second chip 22 and a laminate layer 12 sandwiched between the first and second chips 16 and 22. The laminate layer 12 provides one or more layers of conductive traces separated by insulators and coupled by vias to enable interconnection between the first chip 16, the second chip 22 and external devices (not shown).

The laminate layer 12 includes an upper side 30, a lower side 32 and central passage 14. The central passage may extend along the length of the module 10 in a rectangular arrangement, in one embodiment of the invention.

As shown in Fig. 1, the laminate layer 12 may extend outwardly beyond both of the first and second chips 16 and 22 to form an extension 40. The extension 40 provides a contact surface to make contact with external devices.

The first chip 16 may be coupled to the laminate layer 12 by extending wire bond wires 20 through the central passage 14 to the pads 34 on the upper surface 30 of the laminate layer 12, as shown in Fig. 2. The first chip 16 may be physically coupled to the second chip 22 by an adhesive layer 18. The adhesive layer 18 may conventionally be an adhesive tape strip which adhesively secures the upper surface of the first chip 16 to the lower surface 32 of the laminate layer 12.

The second chip 22 may be coupled to the laminate layer 12 directly using bumps 24 which may be formed of solder balls. As illustrated, the bumps 24 may be of substantially smaller diameter than the bumps 28 provided for connecting the entire module 10 to external devices.

In this way, a relatively low profile multi-chip module may be fabricated. For example, by way of illustration only, in one embodiment of the present invention, the first and second chips 16 and 22 may be on the order of .25 millimeters thick, the laminate layer 12 may be on the order of .25 millimeters thick and the spacing between the first and second chips may be on the order of 0.1 millimeters in the case of the second chip 22

and .075 millimeters in the case of the first chip 16. This gives an overall height of less than one millimeter. If the solder bumps 28 are on the order of .5 millimeters in diameter, the overall height of the assembly may be on the order of about one millimeter, for example .85 millimeter. Thus, a relatively compact, low profile assembly may be fashioned using the winged extension 40.

Referring now to Fig. 2, the sequence of assembling the multi-chip module 10 is illustrated. Initially the first chip 16 is secured by adhesive tape 18 to the lower surface 32 of the laminate layer 12. Wire bond wires 20 extend through the passage 14 to couple the pads 34 on the upper surface 30 of the laminate layer 12 to the first chip 16.

Turning next to Fig. 3, the second chip 22 may be surface mounted on the laminate layer 12 using solder balls 24. After a reflow step, the solder balls 24 soften sufficiently to secure the second chip 22 to be contacts 44 on the upper surface of the laminate layer 12.

Thereafter, the entire assembly is placed in an encapsulation mold, in one embodiment of the present invention, forming the encapsulant 26 in the regions between the first and second chips 16 and 22, as shown in Fig. 4. This leaves the extension 40 extending outwardly from the rest of the package. Alternatively, the gaps

between the chips 16 and 22 may be filled up with underfill material.

For example, in one embodiment of the present invention, solder balls or bumps 28 may be electrically coupled by contacts 52 or 62 to a trace 48 or 58 by way of a via 50 or 60. The traces 48 and 58 in turn may be coupled to each of the contacts 54 or 44 on the upper surface 30 of the laminate layer 12 by way of a via, 56 or 46.

Finally, the solder balls 28 or other interconnection devices are secured to the extensions 40. In this way, external devices may be contacted by the solder balls 28, making electrical connections to the first and second chips 16 and 22 through the laminate layer 12.

Referring to Fig. 5, in one embodiment of the present invention, the extension 40 may extend outwardly from each opposed edges 41 of the module 10. Solder balls 28 may be aligned along each side in the length direction of the extension 40. In some embodiments, each extension 40 may extend outwardly beyond than the approximate width of one solder ball 28 so that a plurality of solder balls may be coupled, two or more solder balls deep, along the edges 41 of the module 10.

Referring to Fig. 6, in accordance with still another embodiment of the present invention, the extension 40 may extend around all four edges 41 of the module 10. In this

way, solder balls 28 may be coupled along four edge portions 41a-d to increase the number of connections that may be made. Again, the extension 40 may extend further outwardly to allow solder balls to be attached, two or more deep, along the edges 41 of the module 10.

While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

What is claimed is: